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9.3.10*

Application number 10/749,910  
Amendment dated May 27, 2009  
Reply to office action mailed February 27, 2009

PATENT

**Amendments to the Specification:**

Please amend the title to read as follows:

**MEMORY SDRAM CONTROLLER HAVING A BUFFER FOR PROVIDING BEGINNING AND END DATA**

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Please replace paragraph [0019] with the following amended paragraph:

[0019] In the illustrated embodiment, the system 10 includes an application-specific integrated circuit (ASIC) 20, which includes various modules 25, such as a processor core (CPU) 27. These modules are interconnected by a bus 30, which may advantageously be an Advanced High-performance Bus (AHB) AHB bus, but which can be any convenient form of bus.

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Please replace paragraphs [0035] and [0036] with the following amended paragraphs:

[0035] Also in step 300, the control logic [[56]] 54 reads the starting address of the request, that is, the address within the SDRAM 40 from which data is first to be retrieved.

[0036] In step 302, the control logic [[56]] 54 determines the requested burst type, i.e., whether a wrapping burst is required. If it is determined in step 302 that a wrapping burst is not required, that is, that an incrementing burst is required, the process passes to step 304. In step 304, the request is processed. It will be appreciated that step 304 does not show in detail the way in which the request is processed, but this can be generally conventional, as understood by a person of ordinary skill in the art. Since a description of this process is not necessary for an understanding of the present invention, a more detailed description is not required.

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Please replace paragraph [0049] with the following amended paragraph:

[0049] As described above, the data from the first SDRAM data burst is stored in the first buffer 60, data from the second data burst is stored in the second buffer 62, and so on, until data from the nth data burst is stored in the nth buffer 64. The SDRAM interface 58 is provided with

enough read buffers that it can store data for the maximum possible fixed length AHB transfer. Each of the read buffers 60, 62, 64 is divided into sub-buffers. For example, Fig. 4 shows sub-buffers 601, 602, 603 in the first buffer 60, sub-buffers 621, 622, 623 in the second buffer 62 and sub-buffers 641, 642, 643 in the [[third]] nth buffer 64. Each of the sub-buffers is able to hold one data beat making up a SDRAM burst.

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Please replace paragraph [0059] with the following amended paragraph:

[0059] Although Figure [[2]] <sup>57</sup> shows the control logic block 554 as being separate from the bus interface blocks 552, 553, some or all of the functionality of the control logic block 554, as described below, can instead be provided in the bus interface blocks.

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Please replace paragraph [0062] with the following amended paragraph:

[0062] Data retrieved from the memory device is returned from the SDRAM interface 558 to the requesting bus interface 552, 553 over a corresponding data line 580, and then stored in the buffers 560, 562, ..., 564 or 570, 572, ..., 574, as the case may be, under the control of the control logic [[556]] <sup>60</sup> 554. The data is then returned to the requesting device from the respective bus interface 552, 553.